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09/868,322	06/18/2001	Yojiro Matsueda	109503	9116

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EXAMINER	
NGUYEN, JENNIFER T	

ART UNIT	PAPER NUMBER
2674	14

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/868,322	Applicant(s) MATSUEDA, YOJIRO
	Examiner Jennifer T Nguyen	Art Unit 2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed on 06/30/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 9-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 9-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to amendment filed on 06/30/2004.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation **"the length of the matrix in a row direction that intersects a column direction along which the plurality of data lines extend being shorter than a length of the display section in the row direction"** in claims 37 and 38 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 9-15, 27-31, 33, 34, and 36-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136) in view of Kumagai et al. (U.S. Patent No. 5,440,718) and further in view of Quanrud (U.S. Patent No. 6,339,417).

Regarding claims 1 and 27, referring to Figs. 47A and 47B, Ikeda teaches a display device, comprising: a display section (2451) having a plurality of scanning lines and a plurality of data lines formed in a grating form corresponding to dots as minimum units of display and active elements provided corresponding to intersections; a scanning line driver (2449) that selects and drives the scanning lines; a memory (2425) having a plurality of memory cells that are capable of storing an image signal for performing display control of dots in at least one row of the display section (2451); a column decoder (2443) that selects the memory cells for storing an input-image signal; a column selection switch section (2445) to switch on the basis of a selection by the column decoder (2443) and the image signal and storing the image signal to said memory cells selected by said column decoder (2443); and a data line driver (2405) that drives

said data lines on the basis of the image signal stored in the memory (2425) (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Ikeda differs from claims 1 and 27 in that he does not specifically teach the plurality of memory cells being arranged in a matrix having a plurality of rows and a plurality of columns and the memory being disposed between the display section and the column selection switch section, and the display section, the memory, and the column selection switch section being formed on one substrate. However, referring to Fig. 1, Kumagai teaches a plurality of memory cells (MC) being arranged in a matrix (i.e., memory cell array 10) having a plurality of rows and a plurality of columns and the memory (10) being disposed between the display section (not shown) and the column selection switch section (12), wherein the memory (10), and the column selection switch section (12) being formed on one substrate (52) (from col. 3, line 64 to col. 4, line 18 and col. 7, lines 18-26) and Quanrud teaches display section, selection switch section and the memory being formed on one substrate (col. 5, lines 12-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the memory cells being arranged in a matrix having a plurality of rows and a plurality of columns and the memory being disposed between the display section and the column selection switch section as taught by Kumagai and the display section, the memory, and the column selection switch section being formed on one substrate as taught by Quanrud in the system of Ikeda in order to provide a driving circuit can be small-sized as a whole, according power consumption in the driving circuit can be reduced.

Regarding claims 9 and 10 Ikeda further teaches the number of the memory cells, which are allocated corresponding to the length in the row direction of said display drive and capable of

storing the image signal for display control of the dots on one row of said display drive, is structured redundantly (col. 33, lines 27-67).

Regarding claims 11, 12, 29-31, Ikeda further teaches on the basis of an address signal representative of a display position and a storage position, said scanning line driver selects the scanning lines and the word line driver selects said word lines (Fig. 1A, col. 9, lines 19-67).

Regarding claim 13, Ikeda further teaches independent address signals are inputted to the scanning line driver and the word line driver (Fig. 1A, col. 9, lines 19-67).

Regarding claims 14, 40, 41, and 43, Ikeda further teaches the scanning line driver operates to select and drive the scanning lines on the basis of the address signal only when a scanning line driver control signal is inputted, and the word line driver operates to select and drive the word lines on the basis of the address signal only when a word line driver control signal is inputted (Fig. 1A, col. 9, lines 19-67).

Regarding claim 15, Ikeda further teaches the column decoder section (2443) selecting the memory cell to store an inputted image signal on the basis of the address signal (from col. 31, line 42 to col. 32, line 58).

Regarding claims 28 and 39, Ikeda further teaches the memory cell section (2425) storing image signals for one screen (2451) (from col. 31, line 40 to col. 33, line 67).

Regarding claims 33, 34, 36, and 42 the combination of Ikeda, Kumagai, and Quanrud teaches the plurality of the memory cell section being configured by a dynamic memory (col. from col. 3, line 64 to col. 4, line 18 of Kumagai).

Regarding claims 37 and 38, referring to Figs. 47A and 47B, Ikeda teaches a display device, comprising: a display section (2451) having a plurality of scanning lines and a plurality

of data lines formed in a grating form corresponding to dots as minimum units of display and active elements provided corresponding to intersections; a scanning line driver (2449) that selects and drives the scanning lines; a memory (2425) having a plurality of memory cells that are capable of storing an image signal for performing display control of dots in at least one row of the display section (2451); a column decoder (2443) that selects the memory cells for storing an input-image signal; a column selection switch section (2445) to switch on the basis of a selection by the column decoder (2443) and the image signal and storing the image signal to said memory cells selected by said column decoder (2443); and a data line driver (2405) that drives said data lines on the basis of the image signal stored in the memory (2425) (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Ikeda differs from claims 37 and 38 in that he does not specifically teach the plurality of memory cells being arranged in a matrix having a plurality of rows and a plurality of columns, the length of the matrix in a row direction extend being shorter than a length of the display section in the row direction, and the memory being disposed between the display section and a selection switch section that control transmission of an image signal to the plurality of memory cells, each of the plurality of memory cells being capable of storing an image signal supplied through the selection switch section, the display section, the memory cell section, and the column selection switch section being formed on one substrate. However, referring to Fig. 1, Kumagai teaches a plurality of memory cells (MC) being arranged in a matrix (i.e., memory cell array 10) having a plurality of rows and a plurality of columns and the memory (10) being disposed between the display section (not shown) and the column selection switch section (12) that control transmission of an image signal to the plurality of memory cells, each of the plurality

of memory cells being capable of storing an image signal supplied through the selection switch section (from col. 3, line 64 to col. 4, line 18 and col. 7, lines 18-26) and Quanrud teaches display section, selection switch section and the memory being formed on one substrate (col. 5, lines 12-20) and it is the matter of design choice to obtain the length of the matrix in a row direction extend being shorter than a length of the display section in the row direction. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the the plurality of memory cells being arranged in a matrix having a plurality of rows and a plurality of columns, the length of the matrix in a row direction extend being shorter than a length of the display section in the row direction, and the memory being disposed between the display section and a selection switch section that control transmission of an image signal to the plurality of memory cells, each of the plurality of memory cells being capable of storing an image signal supplied through the selection switch section, the display section, the memory cell section, and the column selection switch section being formed on one substrate as taught by Kumagai and Quanrud in the system of Ikeda in order to provide a driving circuit can be small-sized as a whole, according power consumption in the driving circuit can be reduced.

6. Claims 16-23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136), Kumagai et al. (U.S. Patent No. 5,440,718) in view of Quanrud (U.S. Patent No. 6,339,417) and further in view of Metegi et al. (6,025,822).

Regarding claims 16 and 17, Ikeda the image signal is inputted on the basis of a unit of one-pixel, and said column decoder selects the memory cell in an amount of one pixel (from col. 17, line 22 to col. 18, line 65). Ikeda differs from claim 16 and 17 in that he does not specifically teach one pixel comprises three dots of developing and display red, blue, and green as light

source colors. However, Motegi teaches one pixel comprises three dots of developing and display red, blue, and green as light source colors (col. 3, lines 11-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the pixel comprises three dots of developing and display red, blue, and green as light source colors as taught by Motegi in the system of Ikeda in order to control the brightness of pixel efficiently.

Regarding claim 18, further Ikeda teaches an input interconnection for the image signal to be stored in the memory cell (2425) and the column selection switch section (2445) are formed on a side opposite to the display drive (2451) sandwiching said memory there between (from col. 31, line 40 to col. 32, line 58).

Regarding claims 19-22, Ikeda further teaches the memory (2425) is allocated with the memory cell corresponding to the length in the row direction of said display drive (2451) and formed in a multi-stage structure (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Regarding claim 23, Ikeda further teaches a timing controller (2409) that controls a timing of transmitting the address signal, and a memory controller (2418) that controls the transmitting of the image signal, the memory controller (2418) being integrated on a semiconductor or an insulating substrate and integrally formed therewith (from col. 31, line 40 to col. 32, line 58).

Regarding claim 25, Ikeda further teaches the display drive (2451) and the memory (2425) are directly coupled to supply the image signal comprising a digital signal stored in the memory (2425) to said display drive (2451) (from col. 31, line 40 to col. 32, line 58).

Regarding claim 26, Ikeda further teaches the display drive performs digital drive through area tonal level (from col. 31, line 40 to col. 32, line 58).

7. Claims 24, 32, 35, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136), Kumagai et al. (U.S. Patent No. 5,440,718) in view of Quanrud (U.S. Patent No. 6,339,417) and further in view of Rao (U.S. Patent No. 5,761,694).

Regarding claims 24, 32, 35, and 44, the combination of Ikeda, Kumagai, and Quanrud differs from claim 24 in that it does not specifically teach a D/A converter is provided between the display drive and the memory cell that converts the image signal comprising a digital signal stored in the memory cell into an analog signal, followed by supplying to the display drive. However, referring to Fig. 1A, Rao teaches a D/A converter (106) is provided between display drive (107) and memory cell (105) that converts the image signal comprising a digital signal stored in the memory cell (105) into an analog signal, followed by supplying to the display drive (107). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the D/A converter is provided between the display drive and the memory cell that converts the image signal comprising a digital signal stored in the memory cell into an analog signal, followed by supplying to the display drive as taught by Rao in the system of the combination of Ikeda, Kumagai, and Quanrud in order to provide a correspond an analog signal to display image successfully.

9. Applicant's arguments with respect to claims 1, 9-44 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jennifer T. Nguyen** whose telephone number is **703-305-3225.** The examiner can normally be reached on Mon-Fri from 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reach at **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to: 703-872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, sixth-floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 703-306-0377.

JNguyen
09/08/2004

REGINA LIANG
PRIMARY EXAMINER